17. (Amended) The virtual address translation module of claim 12, wherein the memory further comprises operational instructions that cause the processing module to utilizing the data when data corresponding to the memory access request is cached.

REMARKS

Applicant respectfully traverses and requests reconsideration.

The specification stands objected to because the acronyms for PCI and GART have not been provided. Applicant has amended the specification to include description of the acronyms as well known in the art.

Claims 2-6 and 13-17 stand rejected under 35 U.S.C. §112 as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter that Applicant regards as the invention. In particular, claims 2, 4 13 and 15 recite the limitation "retrieving a physical page address" and the Office Action alleges that it is not clear where the physical page address is retrieved in the claims. Applicant has amended the recitation (now incorporated in claim 1, for example) which indicates that the physical page address is retrieved based on at least a portion of the virtual address (see, for example, specification page 7, lines 5-7). As such, Applicant respectfully requests that the rejection be withdrawn.

Applicant notes that the only rejection as to claims 4 and 5 were 35 U.S.C. §112 rejections, which Applicant has overcome.

Applicant notes that the claims have been amended to include originally filed dependent claims and as such, the amendments are not narrowing. However, if the Patent Office believes that the amendment is narrowing, Applicant respectfully requests notification of same in writing.

Claim 1 and 12 have been amended to include the respective limitations corresponding, for example, to claims 4 and 5 which indicate that the physical address after a first translation requires further translation and receiving a second physical page address and utilizing the second physical page address and a portion of the virtual address to produce another physical address in that both the first translation and the other second physical address are both stored in the same translation look-aside table.

Claim 7 in the form of a method requires similar steps. As such, Applicant will address reasons why the claims are allowable in view of a combination of the Nakatsuka reference and the Williams reference. For example, claims 3, 7, 14 and 18 stand rejected under 35 U.S.C. §103 as being unpatentable in view of U.S. Patent No. 6,433,782 and U.S. Patent No. 6,199,151. Applicant agrees that the Nakatsuka reference, which is directed to a data processor apparatus and shading apparatus, does not teach, among other things, caching an address in a look-aside table when the address does not correspond to the translation memory space. Moreover, Applicant notes that claim 7 requires translating a virtual address into an address, and caching the address, and also caching another address in the same translation look-aside table corresponding to a translated address, corresponding to a translation memory space. Hence the same look-aside table stores a translated virtual address and also stores a subsequent translation of an address in the same translation look-aside table. Neither of the cited references teach such an operation, alone or in combination. The Office Action cites column 8, lines 66 – column 9, line 39 of Nakatsuka as teaching, among other things, caching another address in the translation look-aside table and wherein the other address is based on an initial virtual address and a translation has already occurred. However, Applicant's respectfully submit that the Nakatsuka reference appears to teach a conventional approach to address translation and simply states in the

cited section that a logical address is converted into a physical address when the data belongs in a particular program region.

The Williams references is directed to an apparatus and method for storing a device row indicator for use in a subsequent page miss memory cycle. Hence, Williams is directed to a mechanism for selecting a row of memory devices and a row value indicates one of plurality of chip select signals that is stored in the storage element that is associated with a first address. A memory access request is received that includes the first address and then one of the plurality of chip select signals indicate by a row value is inserted to select one of the plurality of rows of memory devices. The Office Action cites column 2, lines 43-48 of Williams. However, this portion merely states that when a virtual address causes a translation buffer miss, a physical address is retrieved from a look-up table in a memory sub-system and stored in a translation buffer. The physical address is also processed to identify one of the plurality of device rows. Williams is directed to a completely different system from that of Nakatsuka or that of Applicant's claimed invention. Applicant also submits that the cited portion of Williams merely states that a physical address is retrieved from a look-up table when the virtual address is not on that translation buffer. There is no teaching, among other things, of caching an already translated address in a translation look-aside table, when the address does not correspond to translation memory space, and translating an address into another address when the address corresponds to translation memory spaced and caching the other address in the same translation look-aside table that the first translated address is stored in.

Applicant respectfully submits that the cited references are directed to different problems and hence, do not address the need or present a solution such as does Applicant's claimed invention. For example, each of the references, at best, appears to discuss that a conventional

translation occurs when a virtual address is presented. However, neither of the references indicate, inter alia, to store in the same look-aside table, a translated address from a virtual address and storing a translated address that has been translated based on a previous address in the same translation look-aside table as the first translated address. Accordingly, the claims are in condition for allowance.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "Version with Markings to Show Changes Made."

Applicant respectfully submits that the claims are in condition for allowance and respectfully request that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

By: _____

Christopher J. Reckamp
Reg. No. 34,414

Dated: January 29, 2003

Vedder, Price, Kaufman & Kammholz
222 North LaSalle Street
Chicago, Illinois 60601
Telephone: (312) 609-7599
Facsimile: (312) 609-5005

VERSION WITH MARKINGS TO SHOW CHANGES

In the Specification:

Please replace the paragraph on page 1, beginning at line 17, with the following rewritten paragraph:

Figure 1 illustrates a schematic block diagram of a portion of a computer system. As shown, a central processing unit is coupled to cache memory and to a north bridge. The north bridge is coupled to memory, an accelerated graphics port (AGP) bus, and a peripheral component interconnect (PCI) bus. The central processing unit addresses memory in system virtual address space, or linear address space. To communicate with the north bridge, the central processing unit converts addresses in virtual address space to addresses in physical address space. To make such a conversion, the central processing unit often utilizes page address translation and includes a translation look-aside table (TLB) for storing the conversions.

Please replace the paragraph starting on page 1, beginning at line 26, and continuing to page 2, ending with line 2, with the following rewritten paragraph:

The north bridge, upon receiving an address in physical address space from the central processing unit, determines whether the address corresponds to memory, PCI address space, or AGP memory space. If the address is directed towards the AGP address space, the north bridge makes a further translation of the received physical address utilizing a graphics address relocation table (GART) translation. The translated address is then stored in a GART TLB. As such, for the central processing unit to communicate with the AGP bus, two address space translations occur utilizing separate paging, page address translations and two separate TLBs are maintained.

In the Claims:

Please amend the claims as follows:

Please substitute the following claims for claims having the same number:

1. (Amended) A method for virtual address translation, the method comprises the steps of:

[a)] receiving a memory access request that includes a virtual address;

[b)] determining whether a physical address translation has been performed for the virtual address, wherein the physical address translation translates the virtual address to an address, wherein the address is a physical address of memory or is further translated to obtain another physical address of the memory; [and]

[c)] when the physical address translation or the another physical address translation has been performed for the virtual address, utilizing the physical address or the another physical address to obtain data corresponding to the memory access request;

caching the physical address in a translation look aside table;

when a physical address translation has not been performed for the virtual address, retrieving a physical page address based on at least a portion of the virtual address;

determining whether the physical page address corresponds to a physical address requiring further translation;

when the physical page address does not correspond to a physical address that requires further translation, utilizing the physical page address and a portion of the virtual address to produce the physical address;

when the physical page address corresponds to a physical address that requires further translation, retrieving a second physical page address;

utilizing the second physical page address and a portion of the virtual address to produce the another physical address; and

caching the another physical address in the translation look aside table.

Please delete claims 2, 3, 4 and 5 without prejudice.

6. (Amended) The method of claim 1 [5] further comprises when data corresponding to the memory access request is cached, utilizing the data.

12. (Amended) A virtual address translation module comprises:

a processing module; and

memory operably coupled to the processing module, wherein the memory stores operational instructions that cause the processing module to: [(a)] receive a memory access request that includes a virtual address; [(b)] determine whether a physical address translation has been performed for the virtual address, wherein the physical address translation translates the virtual address to an address, wherein the address is a physical address of memory or is further translated to obtain another physical address of the memory; [and (c)] utilize the physical address or the another physical address to obtain data corresponding to the memory access request when the physical address translation or the another physical address translation has been performed for the virtual address; cache the physical address in a translation look aside table; retrieve a physical page address based on at least a portion of the virtual address when a physical address translation has not been performed for the virtual address; determine whether the physical page address corresponds to a physical address requiring further translation; utilize the physical page

address and a portion of the virtual address to produce the physical address when the physical page address does not correspond to a physical address that requires further translation; retrieve a second physical page address when the physical page address corresponds to a physical address that requires further translation; utilize the second physical page address and a portion of the virtual address to produce the another physical address; and cache the another physical address in the translation look aside table.

Please delete claims 13, 14, 15 and 16 without prejudice.

17. (Amended) The virtual address translation module of claim [16] 12, wherein the memory further comprises operational instructions that cause the processing module to utilizing the data when data corresponding to the memory access request is cached.